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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,295	03/16/2001	Kenneth Rose	M-8372 US	7270
33031	7590	05/20/2005		
CAMPBELL STEPHENSON ASCOLESE, LLP 4807 SPICEWOOD SPRINGS RD. BLDG. 4, SUITE 201 AUSTIN, TX 78759			EXAMINER KHUONG, LEE T	
			ART UNIT	PAPER NUMBER
			2665	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/811,295

Applicant(s)

ROSE, KENNETH

Examiner

Lee Khuong

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— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(e). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 5/22/01.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 1-15 is/are allowed.
- 6) ☒ Claim(s) 16-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to:
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Civanlar et al (US 6,078,963) hereinafter referred as Civanlar.

Regarding claim 16, Civanlar discloses an apparatus of A Router With De-Centralized Processing Using Intelligent Ports. In Civanlar, a routing engine 107, Fig. 1, generates a routing data and transmits a data packet from a source port to a destination port within a switching fabric using the updated routing information comprises:

a buffer (a 1st level cache 209, Fig. 2) configured to receive a data frame (a packet is received at a source port 103A, Fig. 1) to be transmitted to a destination device (to the destination port 103D, Fig. 1) via a first switching fabric (a switching fabric 112, Fig. 2, col. 5, lines 1-13, a packet is received at a source port 103A, which then is stored at a buffer 209. The packet is then forwarded to the switching fabric 112 to be transmitted to a destination device via an output port 103D, Fig. 1),

wherein the first switching fabric comprises data ports (the switching fabric 112, Fig. 1, comprises the data ports 103A-D, Fig. 1) through which data frames enter or exit the first

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switching fabric (see col. 3, lines 60-62, a packet enters at the source port 103A, col. 5, line 2, and exits at the destination port 103D), and

a routing data generation circuit (a routing engine 107, Fig. 1, a routing process 204, Fig. 2) *coupled to the buffer* (the 1st level cache 209, Fig. 2) (see col. 4, lines 43-44, the routing processor 204 is interconnected with the buffer 209 via a high-speed bus 205),

wherein the routing data generation circuit (the routing engine 107) *is configured to generate and add routing data to the data frame received by the buffer* (see Fig. 3, steps 310 and 315, col. 3, lines 28-41, the routing engine 107 generates and updates the routing data contained in routing protocol packets that was received from a network router port 103 and stored in its buffer 209),

wherein the routing data identifies one of the data ports of the first switching fabric through which the data frame will exit to reach the destination device (see col. 8, lines 19-28, the routing data identifies the best egress router port 103, Fig. 1 to reach the destination device via the network interface 110);

wherein the buffer is configured to transmit the received data frame to the switching system after the routing data generation circuit adds the routing data to the data frame (see col. 8, lines 8-11, the switching fabric 112, Fig. 1, comprises ingress data ports and egress data ports. The packet is routed from the 1st level cache 209, Fig. 2, and the routing generated data is inherently added to the packet before transmission).

Civanlar does not disclose expressly a 2nd switching fabric with data ports such that data received from the buffer could be enter and exit from the 2nd switching via its data ports.

Karol discloses a Technique For Internetworking Traffic On Connectionless and Connection-Oriented Networks. In Karol, the CO Switch 410, Fig. 4, is considered as a second switch (see col. 6, lines 35-38) with data ports such that data received (a packet enters at data ports in an input line card 401, Fig. 4) from the buffer (the 1st level cache 209, Fig. 2 of Civanlar) could be enter and exit (a packet exits at data ports in an output line card 402, Fig. 4 from the 1st level cache 209, Fig. 2 of Civanlar, col. 4, lines 36-67)

Civanlar and Karol are analogous art because they are from a similar problem solving area of determining routing data in a switching fabric(es).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the switching fabric of Civanlar with Karol.

The suggestion/motivation for doing so would have been to provide an efficiency of routing through multiple switching fabrics (Karol col. 4, lines 36-67) such that if a routing path via a 1st switching fabric is congested, an alternative path in a second switching fabric is used instead.

Therefore, it would have been obvious to combine Karol with Civanlar to obtain the invention as specified in claim 16.

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Regarding claim 17, please see the rejection of claim 16. The 2nd switch of Karol is to be implemented in Civanlar such that the data received from the cache 209 of Civanlar is to enter the 1st port 103A of 1st switch of Civanlar and exits a port on the output line card on the 2nd switch of Karol.

Regarding claim 18, this claim has similar limitations as claim 16. Therefore, it is rejected under Civanlar and Karol for the same reasons set forth in the rejection of claim 16.

Regarding claim 19, this claim has similar limitations as claim 17. Therefore, it is rejected under Karol for the same reasons set forth in the rejection of claim 17.

Regarding claim 20, this claim has similar limitations as claim 16. Therefore, it is rejected under Civanlar and Karol for the same reasons set forth in the rejection of claim 16.

Regarding claim 21, this claim has similar limitations as claim 16. Therefore, it is rejected under Karol for the same reasons set forth in the rejection of claim 16.

Allowable Subject Matter

3. Claims 1-15 are allowed.

Reason for Allowance

4. The following is a statement of reasons for the indication of allowable subject matter:

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Regarding claims 1-15, the prior art fails to teach or suggest a method comprising two switching fabrics that comprises the steps of concatenating the second multi-bit value with itself to produce a concatenated second multi-bit value and bit wise logically ANDing the selected first multi-bit value with the concatenated second multi-bit value to produce a third multi-bit value, wherein the third multi-bit comprises concatenated first and second portions, in combination with other limitations, as specified in the independent claims 1 and 9.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

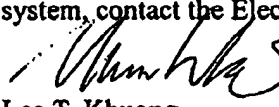
Blanc et al (US 6,597,656); Sethu (US 5,812,549) are cited to show system and method for providing Hardware Load Balancing Through Multiple Fabrics, which is considered pertinent to the claimed invention.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lee Khuong whose telephone number is 571-272-3157. The examiner can normally be reached on 9AM - 5PM.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Lee T. Khuong
Examiner
Art Unit 2665

DUCHO
PRIMARY EXAMINER


11-22-04

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